

MR252xx

(CU and CC)

Camera Core

Specification

February 26, 2008

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2 Revision History

Revision	Date	Who	What
0.10	19.05.2007	ML	Initial draft created from MR282. Updated with CCD vs. housing tolerances, quantum efficiency, power consumption, storage and transportation environments, absolute maximum operation conditions
0.20	06.07.2007	ML	Updated refresh rates and resolutions
1.00	26.02.2008	ML	Modes table updated, VPP references changed to CTP, optical path specs added, release

3 Disclaimers

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4 Privacy Information

This document contains information of a sensitive nature. This information should not be given to persons other than those who are involved in the MR252 project or who will become involved during the lifecycle.

5 Trademarks

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6 Glossary of Terms, Acronyms and Abbreviations

ADU	Analog to Digital Units
API	Application Program Interface
CCD	Charge Coupled Device
CTP	Compliance Test Procedure
DDRAM	Dual Data rate Random Access Memory
DLL	Dynamic Link Library
FPGA	Field Programmable Gate Array
FWC	Full Well Capacity
GUI	Graphical User Interface
OHCI	Open Host Controller Interface
PC	Personal Computer
PCB	Printed Circuit Board

7 Document Scope and Purpose

The purpose of this document is to specify MR252 camera core parameters and their dependencies.

8 Referenced Documents

- MR252 Compliance Test Procedure (MR252CTP)
- MR252 Validation and Verification Plan (MR252VVP)
- Sony datasheet E00109-PS

9 Parameter tables

9.1 Mechanical

Description	Symbol	Value	Units
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Height	H	32	mm
Width	W	60	mm
Depth	D	60	mm
Weight	M	100	g
Alignment of CCD chip sensitive area relative to the housing		±0.25	mm
Housing material and technology		Machined Aluminium alloy, no further surface treatments	
Lens adapter, material and technology		C-Mount, machined Aluminium alloy, anodized to black color	

9.2 Sensor

Description	Symbol	Value	Units
Brand		Sony ICX252AQ	
Type		Frame readout CCD image sensor, 2 fields	
Pixel resolution		2048 (H) × 1536 (V)	pixels
Chip size		8.10(H) x 6.64(V)	mm
Unit cell size		3.45(H) x 3.45(V)	µm
Color filter		RGB Bayer mosaic	
FWC (*), typical		10000	ē
Dark current (**), typical		9	ē/p/s

All parameters in this table, except FWC and Dark current, are reprinted from Sony datasheet E00109-PS

(*) – FWC, no limits specified by CCD chip vendor, typical value provided here is for informational purposes only. It can not be used as a unit qualification parameter.

(**) – Dark current, limit specified by CCD chip vendor is ~200ē/p/s. A typical value provided here is for informational purposes only. It can not be used as a unit qualification parameter.

9.3 Optical path

Description	Symbol	Value	Units
IR Filter Brand		Hoya E-CM500S	
Thickness		1.0±0.1	mm
Specification		HOYA 8405E	
Coating		NA	
CCD Spot blemishes and stain specification		Sony E02X24	
Filter cleanness (spots, scratches)		±3 (*)	%
Size of the cosmetics defects free aperture on filter		21.5	mm

(*) – Filter cleanness is measured with the method and set of tools described in MR252CTP.

9.4 Camera core

Description	Symbol	Value	Units
Digitization		14	Bit
Supported bit resolutions		8, 10, 12 and 14	Bit/pix
Exposure time		20µs ... 500sec	
Variable Gain Range	VGA	36	dB
Refresh rate	MRR	7.1	Fps
Trigger/sync input (r)		Asynchronous CMOS 3.3V	
Trigger/sync output (rr)		CMOS 3.3V	
Dynamic range, Typical		>58	dB
Linearity (*)		<1	%

Acquisition Gain (14bit)		2.4 ±0.5	ē/ADU
Lens adapter		C-Mount	
External interface		IEEE1394A	
Acquisition noise (**), typical		1.3	ADU
Acquisition noise (**), max		2.0	ADU
Readout noise (***), typical		3.5	ADU
Readout noise (***), max		NA	ADU

All parameters in this table are subject to qualification measurements specified in MR252CTP and Sony data sheet E00Z37-PS

(r) – Pull up resistor of 100kΩ

(rr) – Serial resistor of 1kΩ

(*) – Linearity of 1% guaranteed in the range of exposures 1ms to 16s.

(**) – Acquisition noise means noise generated by the camera with ADC input connected to ground via resistor equivalent to CCD output impedance of 200Ω.

(***) – Readout noise means noise generated by the camera with ADC input connected to CCD chip. Typical value provided here is for informational purposes only. It can not be used as a unit qualification parameter.

9.5 Power

Description	Symbol	Value	Units
Power supply, via IEEE1394 system connector	V _{nom}	12 ±10%	V
Consumption, typical no cooling	P _{nom}	1.5	W
Consumption, maximum no cooling	P _{max}	2.2	W
Consumption, typical cooling on (MR252CC only)	P _{nom-cool}	3.2	W
Consumption, maximum cooling on (MR252CC only)	P _{max-cool}	5.0	W

All parameters in this table are subject to qualification measurements specified in MR252CTP

9.6 Cooling performance (MR252CC only)

Description	Symbol	Value	Units
Lowest possible temperature on the CCD chip	T _{chip}	10	°C
Housing temperature accuracy	T _{h-acc}	2	°C
CCD chip temperature accuracy	T _{c-acc}	3	°C
Maximum achievable temperature difference between housing and chip	T _{diff}	26	°C

All parameters in this table are subject to qualification measurements specified in MR252VVP

9.7 Environment

Description	Symbol	Value	Units
Ambient temperature operation	T _{norm}	+10 ... +25	°C
Absolute maximum of ambient temperature operation (*)	T _{max}	+5 ... +60	°C
Ambient temperature for storage and transportation	T _{storage}	-25 ... +70	°C
Relative Humidity, non condensing	RH	80	%

All parameters in this table are subject to qualification measurements specified in MR252VVP

(*) – Housing temperature shall not exceed +65°C, also beyond of the optimal range the following parameters are not guaranteed:

Dark current, Dynamical Range, Linearity, Acquisition and readout noise, S/N ratio, cooling performance (MR252CC only), durability.

9.8 Firmware/Host driver/API features

Description	Symbol	Value	Units
Interpolation method		9331, SHT_advanced	
White balance coefficients ranges		0.0 ... 3.9	x
Sharpness filter		0 ... 100	%
Gamma		0.3 ... 1.0	
Full color correction matrix (3+1)x3 coefficients ranges		-3.9 ... 3.9	x
Partial readout granularity @ (1x binning)		2 (H) x 2 (V)	pixels
Max refresh rate x1 binning (intrl)		14.1	Fields/s
Max refresh rate x2 binning (intrl)		27.2	Fields/s
Max refresh rate x4 binning (intrl)		50.0	Fields/s

All parameters in this table are subject to qualification measurements specified in MR252VVP

9.9 Supported readout modes

Mode	Binning	Scan	Mode	Pixels	Frames/s	Fiedls/s
0	2x2	Progressive HS	B/W	1040 (H) × 772 (V)	27.1	NA
1	1x1	Interlace 1L	Color	2080 (H) × 1544 (V)	7.1	14.1
2	2x2	Interlace	Color	1040 (H) × 772 (V)	13.6	27.1
3	3x3	Interlace HS	Color	688 (H) × 514 (V)	35	70
4	2x2	Interlace HS	Color	1040 (H) × 772 (V)	25	50
5	2x2	Progressive	B/W	1044 (H) × 774 (V)	14	NA
6	1x1 (*)	Interlace HS	Color	2088 (H) × 1550 (V)	12.5	25
7	3x3	Interlace HS	Color	696 (H) × 516 (V)	19.5	39
8	4x4	Interlace HS	Color	522 (H) × 386 (V)	45	90
9	4x4	Interlace	Color	522 (H) × 386 (V)	25	50
10	6x6 skip	Progressive	Color	348 (H) × 258 (V)	39	NA
11	6x6 skip	Progressive HS	Color	348 (H) × 258 (V)	70	NA

(*) – only 8bpp mode supported

All parameters in this table are subject to qualification measurements specified in MR252VVP